Amendments to the Specification:

In the Specification:

Please replace paragraph [0017] with the following new paragraph [0017]:

[0017] Fig. 1 is a block diagram representing an FRC-enabled processor 110. Processor 110 includes first and second execution cores 120(a), 120(b) (generically, execution core 120), an FRC checker 130, an error detector 140, a recovery unit 150, and reset unit 160. A portion of the FRC-boundary is indicated by dashed line 104. For purposes of illustration, recovery unit 150 and reset unit ~~170~~ 160 are shown as part of processor 110, but portions of these units may be implemented as firmware or software modules that are located off of the processor die.

Please replace paragraph [0024] with the following new paragraph [0024]:

[0024] Each execution core 220 includes a data pipeline 224 and an error pipeline 228 that feeds into FRC checker 230 and error detector ~~140~~ 240, respectively. Execution cores 220(a), 220(b) and their components operate in substantially the same manner as described above for execution cores 120(a), 120(b).

Please replace paragraph [0025] with the following new paragraph [0025]:

[0025] Error detector 240 monitors error pipelines 228(a), 228(b). If a signal or flag indicates an error in one of execution cores 220, error detector 240 disables FRC checker 230 and activates recovery unit 250. As discussed below in greater detail, FRC checker ~~240~~ 230 provides buffering that allows error detector ~~230~~ 240 to activate recovery unit 250, even if it detects the error after FRC checker 230 detects a mismatch

between the corresponding corrupted and uncorrupted data. Provided the error is detected within a countdown interval initiated by an FRC mismatch, the FRC mismatch is ascribed to the error, and processor 210 activates a recovery routine through recovery unit 250 rather than a slower reset routine through reset unit 260.

Please replace paragraph [0031] with the following new paragraph [0031]:

[0031] For the instant reflected in Fig. 3A, data_0 has been accepted and forwarded to queue ~~338~~ 336 for further processing. Here, "accepted" means that the data_0 blocks provided by master and slave execution cores 320(a), 320(b), respectively, matched, and no FRC error is indicated by comparator 370. Data_1 through data_3 are accepted and currently stored in buffer entries 380(1)-380(3), awaiting transfer to queue ~~338~~ 336. Data_4 through data_8 are currently propagating through data pipelines ~~224(a)~~ 324(a), ~~224(b)~~ 324(b) of master and slave execution cores, ~~220(a)~~ 320(a), ~~220(b)~~ 320(b), respectively. An error associated with data_4 in data pipeline 324(a) (indicated by dashed line) is propagating through error pipeline 328(a) approximately two clock cycles behind data_4. For example, the error may represent a 2-bit soft error detected by ECC hardware. The detection hardware for 2-bit ECC errors is relatively complex, and may contribute to the delay indicated between data_4 and its error flag.

Please replace paragraph [0032] with the following new paragraph [0032]:

[0032] Fig. 3B shows processor 310 at a later instant in which data_3 from execution core 320(a) has been forwarded to queue 336, data_4 - data_6 have been transferred to buffer 380 and their match status determined. In particular, comparator 370 has signaled a mismatch (reject) for data_4, which was corrupted by a soft error, and its uncorrupted counterpart from execution core 320(b). Comparator 370 has also

triggered the stall signal to slave execution core 320(b) and triggered timer unit 338 to begin the countdown interval. For the disclosed embodiment, stalling one of data pipelines 324 ensures that an uncorrupted copy of the data is preserved for recovery unit ~~360~~ 350, in either the stalled pipeline or compare/buffer unit 334.

Please replace paragraph [0034] with the following new paragraph [0034]:

[0034] During the countdown interval, error detector 340 also continues to track flags from error pipelines 328. If the error flag associated with data_4 reaches error detector 340 before timer unit 338 signals the end of the countdown interval, error detector 340 disables FRC checker 330 and activates recovery unit ~~360~~ 350. If timer unit 338 detects the end of the countdown interval before error detector 340 detects the error flag, reset unit ~~370~~ 360 is activated.

Please replace paragraph [0035] with the following new paragraph [0035]:

[0035] Figs. 4A and 4B are block diagrams of another embodiment of a processor 410 in accordance with the present invention at two different times. Contents of data pipeline 424 and error pipeline 428 are labeled to indicate the relative times at which they are processed through execution core 420. For processor 410, the disclosed embodiment of compare/buffer 434 includes a comparator 470 and buffer entries 480(1)-480(3) (generically, buffer entries 480). Comparator 470 compares data from execution cores 420(a) and 420(b) and generates a match status signal according to the comparison. Each buffer entry 480 includes data fields ~~384~~ 484 and ~~388~~ 488 to store data from execution cores 420(a) and 420(b), respectively, and a status field 486 to store the status determined by comparator 470.

Please replace paragraph [0036] with the following new paragraph [0036]:

[0036] For system 400, data blocks from both pipelines 424(a), 424(b) are transferred to FRC checker 430. Consequently, no stall signal is needed to preserve uncorrupted data in one of execution cores 420 following detection of an FRC mismatch by comparator 470. The uncorrupted data may be provided from the appropriate entry of buffer 480.

Please replace paragraph [0037] with the following new paragraph [0037]:

[0037] Timer unit 438 initiates a countdown interval in response an FRC mismatch detected by comparator 470. FRC checker 430 and error detector 440 continue to process data and flags, respectively, during the countdown interval. If an error reaches error detector 440 before the countdown interval expires, error detector 440 disables FRC checker 430 and activates recovery unit ~~460~~ 450. If the countdown interval expires first, FRC checker 430 activates reset unit ~~470~~ 460 to reset system 400.

Please replace paragraph [0042] with the following new paragraph [0042]:

[0042] Fig. 6 is a block diagram representing one embodiment of a computer system 600 in which the present invention is implemented. The disclosed embodiment of system 600 includes a processor 610, chipset ~~670~~ 682, main memory 680, non-volatile memory 690 and peripheral device(s) ~~694~~ 698. Chipset ~~670~~ 682 manages communications among processor 610, main memory 680, non-volatile memory 690 and peripheral devices ~~694~~ 698.

Please replace paragraph [0044] with the following new paragraph [0044]:

[0044] Error check units 630(a), 630(b) (generically, error check units 630) compare results from execution cores 620 before they are transferred to shared resources like cache 640 and FSB 660. They thus form part of the FRC boundary of processor 610. Each error check unit 630 includes an FRC checker 230 and error detector 240 (Fig. 2) to provide FRC and non-FRC error checking/detection, respectively, for execution cores 620. Error check units 630 may also include portions of recovery unit ~~240~~ 250 and reset unit 260 (Fig. 2). For one embodiment of system 600, a recovery routine 692 and a reset routine 694 may be stored in non-volatile memory 690 and images of these routines may be loaded in main memory 680 for execution. For this embodiment, recovery unit ~~240~~ 250 and reset unit 260 may include pointers to recovery routine 692 and reset routine 694, respectively (or their images in main memory 680).